TPS720xxEVM-307

This user's guide describes the characteristics, operation, and use of the TPS720xxEVM-307 evaluation module (EVM). This EVM demonstrates the Texas Instruments TPS720xx tiny low dropout (LDO) linear regulator in a 5-pin WCSP package. The TPS720xx supplies up to 350 mA of output current at a fixed output voltage from a 1.1 V to 4.5 V input source. This user's guide includes setup instructions, test results, schematic diagram, bill of materials (BOM), and PCB layout drawings for the EVM.

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1 Introduction

The TPS720xxEVM-307 evaluation module (EVM) assists designers in evaluating the operation and performance of the TPS720xx low dropout (LDO) linear regulator. This LDO provides up to 350 mA of output current at a fixed output programmed at the factory. The board features the 1,33-mm × 0,96-mm 5-pin WCSP package for a tiny solution size.

1.1 Related Documentation From Texas Instruments

TPS720xx, 350 mA Low Dropout Linear Regulator with Bias Pin in a 5-Pin WCSP Package data sheet (SBVS100)

1.2 Performance Specification Summary

Table 1 provides a summary of the TPS720xxEVM-307 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Typical Performance Specification Summary

	CONDITION	VOLTAGE RANGE (V)			CURRENT RANGE (mA)		
		MIN	TYP	MAX	MIN	TYP	MAX
V_{BIAS} supply	TPS72013EVM-307 (HPA307-001)	2.7(1)		5.5			5
	TPS72015EVM-307 (HPA307-002)	2.9(1)		5.5			5
V_{IN} supply	TPS72013EVM-307 (HPA307-001)	1.5(1)		4.5V or V_{BIAS}(2)(3)			350
	TPS72015EVM-307 (HPA307-002)	1.7(1)		4.5V or V_{BIAS}(2)(3)			350
V_{OUT}	TPS72013EVM-307 (HPA307-001)	1.274	1.3	1.326			350(2)
V_{OUT}	TPS72015EVM-307 (HPA307-002)	1.47	1.5	1.53			350(2)

(1) This is the minimum voltage to provide the maximum output current in the table assuming the typical V_{BIAS} voltage is applied. Lower output currents are achievable with lower V_{IN} and V_{BIAS} voltages. See the data sheet for V_{IN} to V_{OUT} and V_{BIAS} to V_{OUT} dropout data.

(2) Linear regulator power dissipation is computed as $P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$. As specified in the data sheet, the regulator's package has a finite power dissipation rating depending on the ambient temperature, board type, and airflow. Using V_{IN} and/or V_{OUT} voltages other than the typical voltages recommended in the table or using the EVM in an environment with an ambient temperature higher than 25°C significantly reduces the maximum allowed output current. See the data sheet for the regulator package's thermal resistance data, and see TI application report *Digital Designer's Guide to Linear Voltage Regulators and Thermal Management* (SLVA118) for a full explanation.

(3) The maximum allowable voltage on V_{IN} is the lesser of 4.5V or the voltage on V_{BIAS}, as specified in the datasheet.

1.3 Modifications

To aid user customization of the EVM, the board was designed with devices having 0603 or larger footprints. A real implementation likely occupies less total board space.

Changing components can improve or degrade EVM performance. For example, adding a larger output capacitor reduces output voltage undershoot but lengthens response time after a load transient event. Adding a larger input capacitor reduces droop at the V_{IN} pin that inductive leads from the V_{IN} power supply may cause during a load transient.

2 EVM Jumpers and Connectors

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS720xxEVM-307.

Table 2. TPS720xxEVM-307 Jumpers and Connectors

JUMPER	DESCRIPTION	DIRECTIONS
J1 - pin 1	Input Bias Voltage Connection	Connect the lead from the power terminal of the bias input source to this input. The supply must be between 2.5 V and 5.5 V. The supply must also be at least 1.4 V above the output voltage.
J1 - pin 2	Input Bias Ground Connection	Connect the lead from the return terminal of the bias source to this input.
J2	Input V_{IN} Connection	Connect the lead from the power terminal of the input source to this input. The supply must be between 1.1 V and 4.5 V. The supply must be greater than 200 mV plus the output voltage.
J3	Input Ground Connection	Connect the lead from the return terminal of the input source to this input.
J4	Output V_{OUT} Connection	Connect the positive side of the load and/or output multimeter to this output.
J5	Output Ground Connection	Connect the lead from the return terminal of the load and/or output multimeter to this output.
JP1	V_{IN} and V_{BIAS} Connection	This jumper allows the user to use one supply to power the TPS720xxEVM-307. Place a shunt across the pins of JP1 to connect the V_{IN} and V_{BIAS} inputs. The J1 or the J2 connector may be used to supply the circuit with the shunt installed. In this mode, the supply must meet the requirements for both the V_{IN} and V_{BIAS} supplies. Remove the shunt to use separate supplies for each input.
JP2	EN	Enable input for the TPS720xxEVM-307. Place a shunt across the ON and EN pins of JP2 to enable the TPS720xxEVM-307. Place a shunt across the OFF and EN pins of JP2 to disable the TPS720xxEVM-307. A shunt must be installed on JP2 in either ON or OFF positions and EN should not be left unconnected.

3 Operation

Connect the positive input of the bias supply to the V_{BIAS} pin on J1 (pin 1). Connect the positive input power supply to the V_{IN} pins on J2. Connect the input bias supply return (ground) to pin 2 of J1. Connect the input power return (ground) for V_{IN} to the GND pin on J3. The TPS720xxEVM-307 has a maximum input voltage of 5V for V_{IN} and 6V for V_{BIAS}. The recommended maximum operating input voltage is 4.5 V for V_{IN} and 5.5V for V_{BIAS}.

Connect the desired load between V_{OUT} (J4) and GND (J5). The TPS720xx supplies up to 350 mA of output current.

Configure jumpers JP1 and JP2 as described in the TPS720xxEVM-307 Jumpers and Connectors table.

4 Test Results

This section provides typical performance waveforms using the TPS720xxEVM-307 printed circuit board.

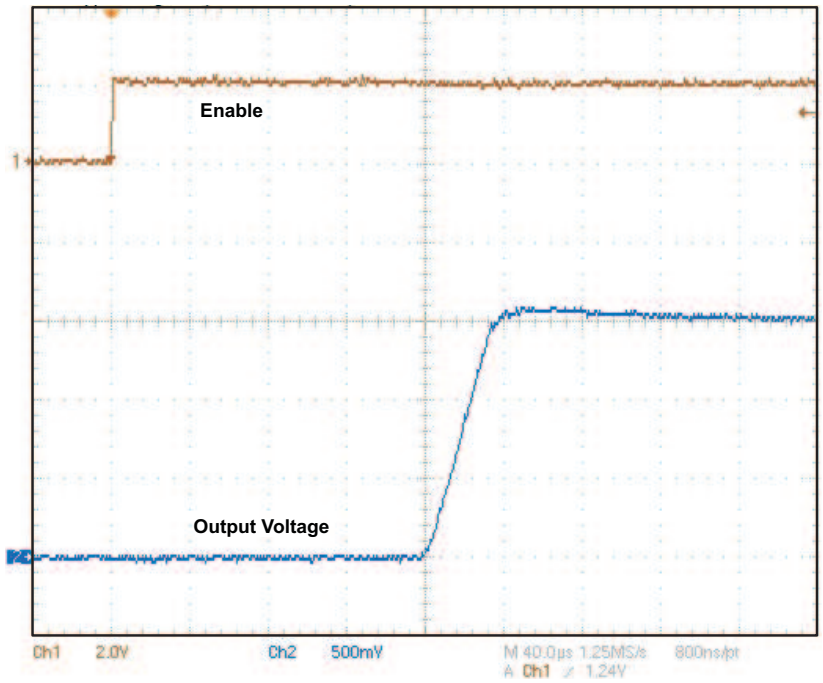


Figure 1. Startup From Enable of the TPS72015EVM-307 into 350 mA Load (V_{IN} = 2V, V_{BIAS} = 2.9V)

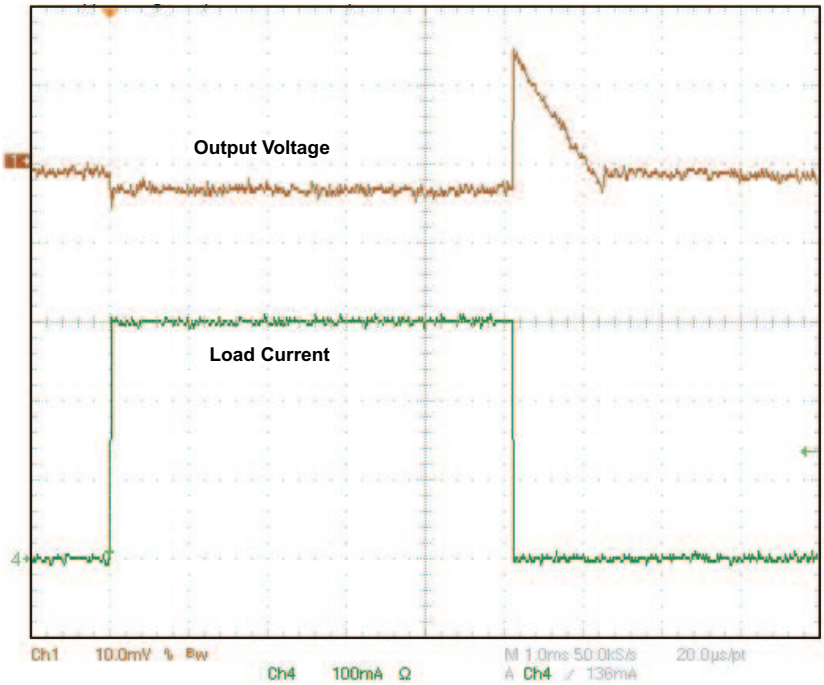


Figure 2. Load Transient of the TPS72015EVM-307, V_{IN} = 2V, V_{BIAS} = 2.9V, I_{OUT} = 0mA to 300mA to 0mA

5 Board Layout, Schematic and Bill of Materials

This section provides the TPS720xxEVM-307 board layout, schematic and bill of materials.

5.1 Board Layout

Board layout is important for all LDO power supplies. If the layout is not carefully done, the regulator could show stability problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input and output capacitor should be placed as close as possible to the IC. Figure 3 through Figure 5 show the board layout for the TPS720xxEVM-307 PCB.

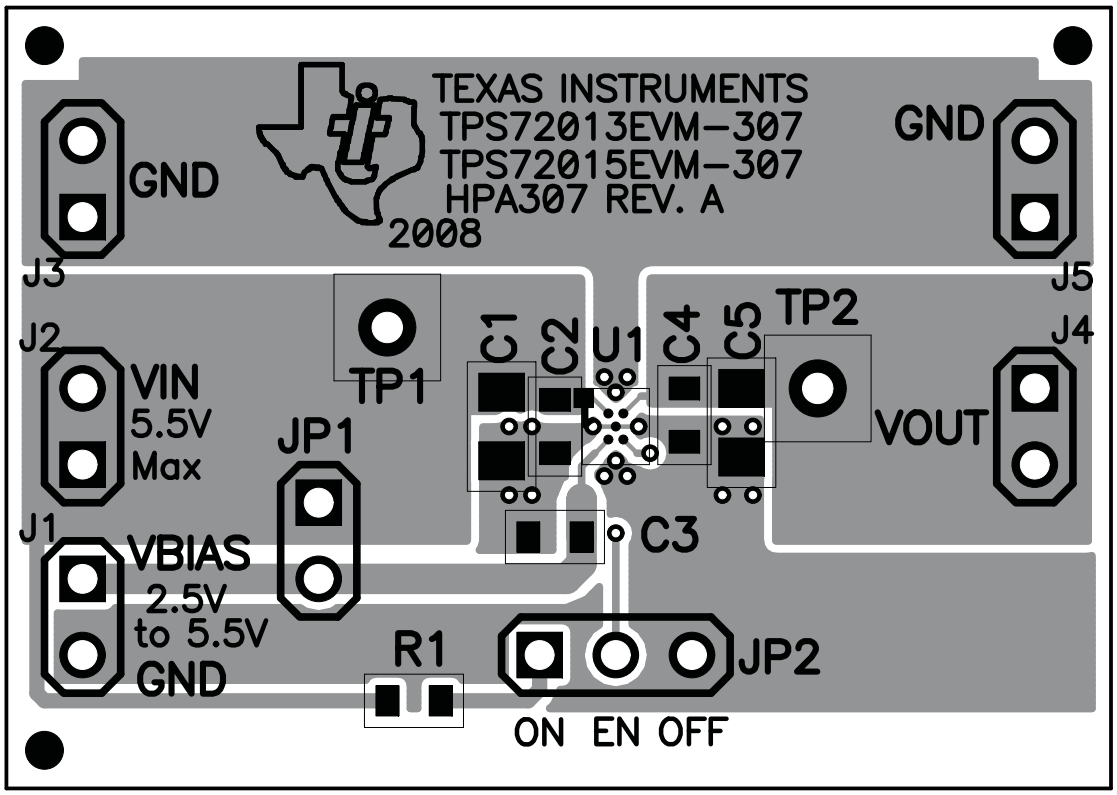


Figure 3. Top Assembly Layer

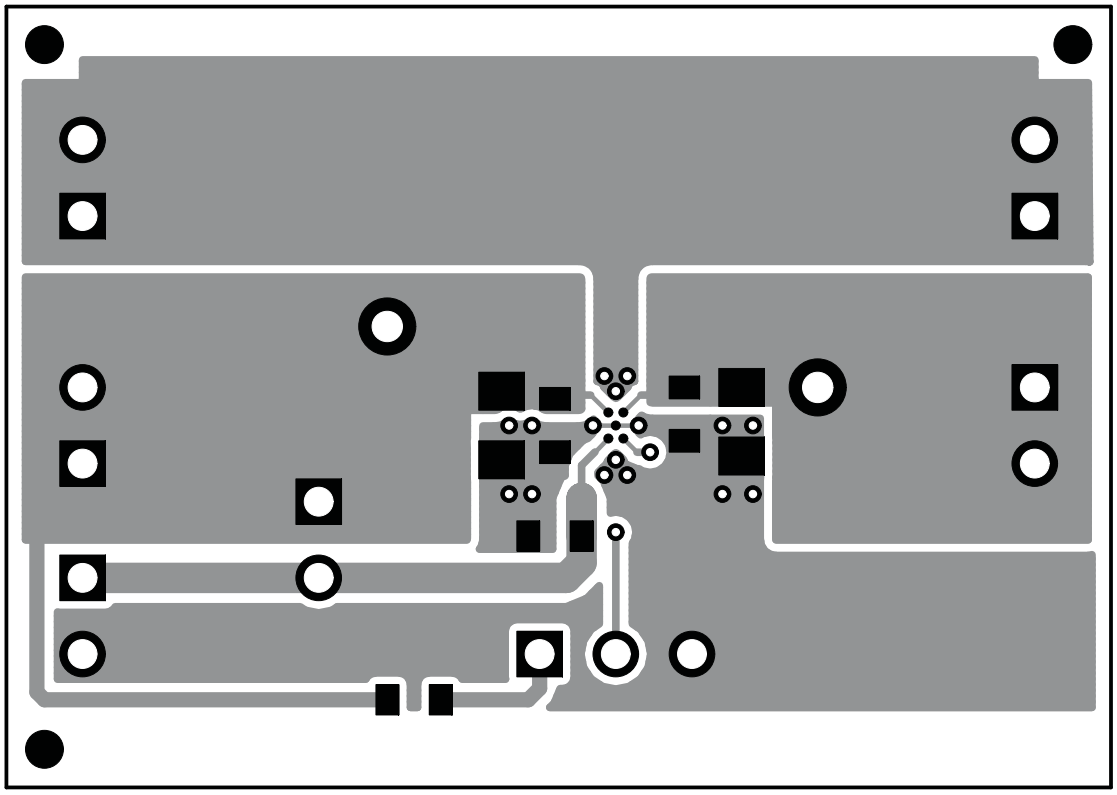


Figure 4. Top Layer

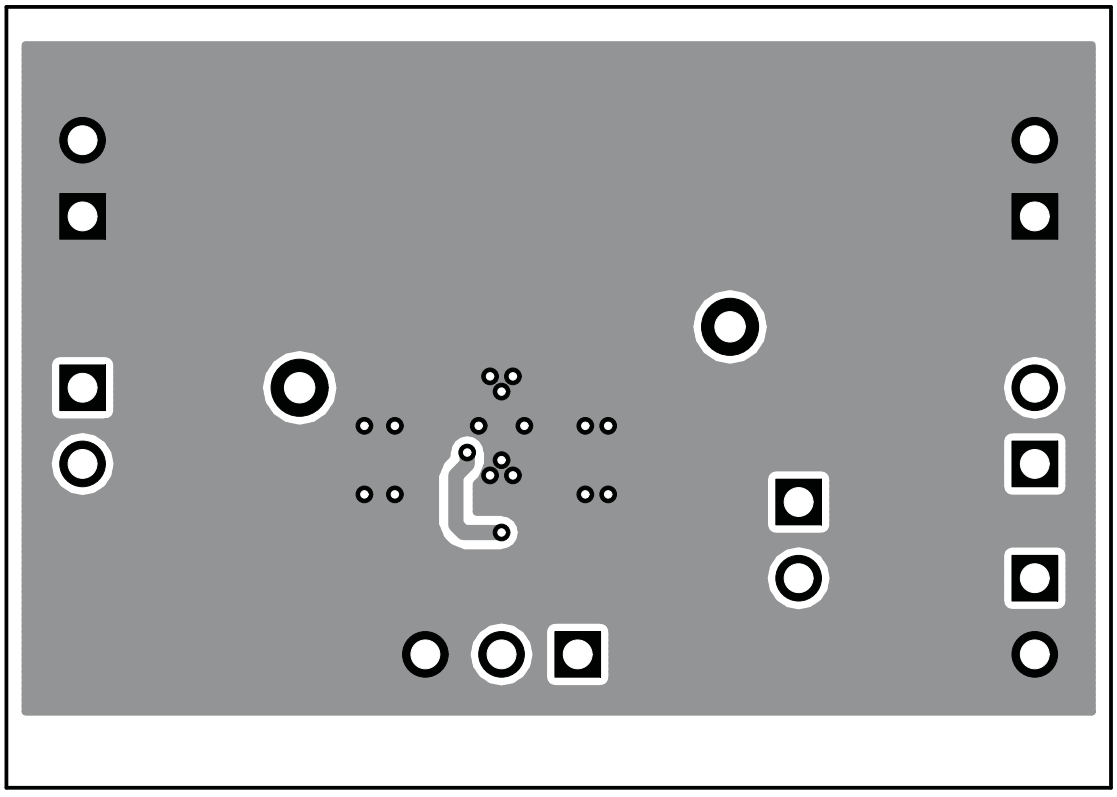


Figure 5. Bottom Layer

5.2 Schematic and Bill of Materials

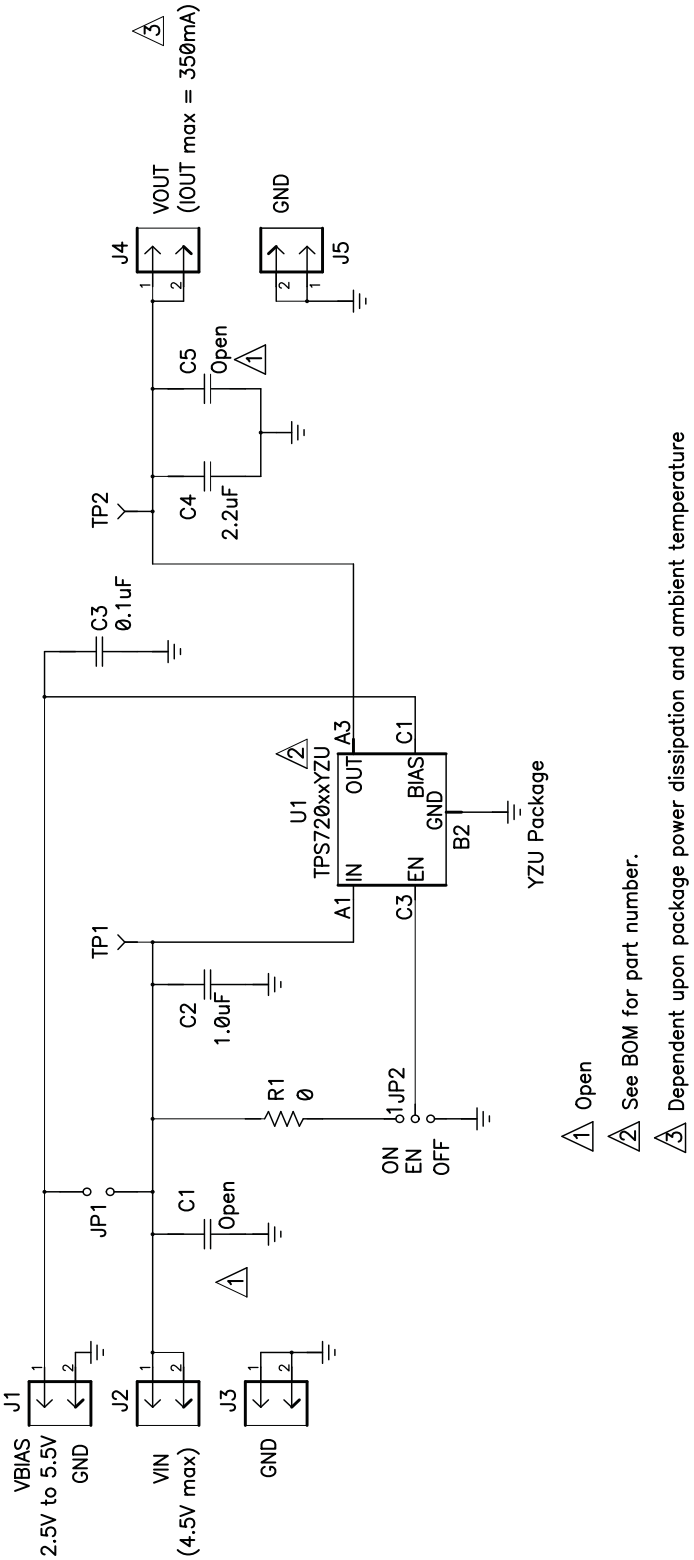


Figure 6. TPS720xxEVM-307 Schematic

Table 3. Bill of Materials

COUNT		RefDes	Value	Description	SIZE	Part Number	MFR
-001	-002						
0	0	C1	Open	Capacitor, Ceramic, 10V, X5R, 20%	0805	Std	Std
1	1	C2	1.0uF	Capacitor, Ceramic, 10V, X5R, 20%	0603	Std	Std
1	1	C3	0.1uF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	Std	Std
1	1	C4	2.2uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	Std	Std
0	0	C5	Open	Capacitor, Ceramic, 6.3V, X5R, 10%	0805	Std	Std
1	1	R1	0	Resistor, Chip, 5%	0603	Std	Std
5	5	J1- J5	PTC36SAAN	Header, Male 2-pin, 100mil spacing, (36-pin strip)	0.100 inch x 2	PTC36SAAN	Sullins
1	1	JP1	PTC36SAAN	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 inch x 2	PTC36SAAN	Sullins
1	1	JP2	PTC36SAAN	Header, 3-pin, 100mil spacing, (36-pin strip)	0.100 inch x 3	PTC36SAAN	Sullins
2	2	TP1, TP2	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
1	0	U1	TPS72013YZU	IC, LDO Linear Regulator With Bias Pin, 350mA	WCSP-5	TPS72013YZU	TI
0	1		TPS72015YZU	IC, LDO Linear Regulator With Bias Pin, 350mA	WCSP-5	TPS72015YZU	TI
2	2	–		Shunt, 100mil, Black	0.1	929950-00	3M
1	1	–		HPA307 Rev. A PCB	0.062"x1.025"x1 .45"	HPA307	Any

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 1.1 V to 4.5 V on Vin and 2.5 V to 5.5V on Vbias and the output voltage range of 0.9 V to 3.6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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